

IN THE DRAWING:

Please add new Figure 16, attached hereto.

IN THE CLAIMS:

3  
B  
1 ~~152~~<sup>2</sup>. (Amended) The synchronous memory device of claim ~~151~~<sup>1</sup>  
2 further including output drivers, coupled to an external bus, to  
3 output data on the bus, in response to the read request,  
4 synchronously with respect to an external clock [wherein the value  
5 which is representative of the delay time is stored in the register  
6 after power is applied to the device].

1 ~~153~~<sup>3</sup>. (Amended) The synchronous memory device of claim [151]  
2 ~~152~~<sup>2</sup> wherein the value [which] is representative of a number of  
3 clock cycles of the external clock [the delay time is stored in the  
4 register after the memory device is reset].

1 ~~154~~<sup>4</sup>. (Amended) The synchronous memory device of claim ~~151~~<sup>1</sup>  
2 wherein, during an initialization sequence, the programmable  
3 register stores the value [which is representative of a delay time  
4 is stored in the register when the memory device is initialized].

C  
1 ~~155~~<sup>5</sup>. (Amended) The synchronous semiconductor memory device of  
2 claim ~~151~~<sup>1</sup> wherein, in response to a <sup>control register access</sup> ~~set register request~~, the

3 programmable register stores the value [which is representative of  
4 a delay time is stored in the programmable register].

[ In claim 157, line 7 insert --a-- before "first."

11.1  
1 ~~161.~~ (Amended) The synchronous semiconductor memory device of  
2 claim ~~157~~ wherein, during an initialization sequence, the  
3 programmable register stores the value [which is representative of  
4 the programmable delay time is stored in the programmable register  
5 after the memory device is initialized].

14.1  
1 ~~164.~~ (Amended) A synchronous semiconductor memory device  
2 having at least one memory section which includes a plurality of  
3 memory cells, the memory device comprising:

BS  
4 a programmable register to store a value which is  
5 representative of a number of clock cycles of an external clock to  
6 transpire before data is output onto an external bus in response to  
7 a read request [delay time after which the memory device responds  
8 to a read request]; and

9 a plurality of output drivers, coupled to the bus, to output  
10 data in response to the read request, wherein the output drivers  
11 output data on [a] the bus after the number of clock cycles of the  
12 external clock transpire [in accordance with the delay time].

1 <sup>15</sup>  
~~165.~~ (Amended) The synchronous memory device of claim <sup>14</sup>~~164~~  
2 wherein the value [which] is representative of a fraction or a  
3 whole number of clock cycles of the external clock [the delay time  
4 is stored in the register after power is applied to the device].

1 <sup>16</sup>  
~~166.~~ (Amended) The synchronous memory device of claim <sup>14</sup>~~164~~  
2 wherein, during an initialization sequence, the programmable  
3 register stores the value [which is representative of a delay time  
4 is stored in the register when the memory device is initialized].

1 <sup>17</sup>  
~~167.~~ (Amended) The synchronous semiconductor memory device of  
2 claim <sup>14</sup>~~164~~ wherein, in response to a control register access  
3 programmable register stores the value [which is representative of  
4 a delay time is stored in the programmable register].

1 <sup>18</sup>  
~~168.~~ (Amended) A method of controlling the operation of a  
2 synchronous semiconductor memory device wherein the memory device  
3 includes a register, the method comprising:  
4 providing a time delay value to the memory device;  
5 storing [a] the time delay [time-delay] value in the register  
6 in the memory device, wherein the time delay [time-delay] value is  
7 [being] representative of a time delay after which the memory  
8 device responds to a transaction request.

In claim 174, on line 1, delete "the step of".

Please **add** the following claims:

1 <sup>27</sup>~~177~~. A method of operation of a semiconductor memory device  
2 wherein the memory device includes a programmable register, the  
3 method comprising:  
4 receiving a time delay value, wherein the time delay value is  
5 representative of a number of clock cycles of an external clock to  
6 transpire before data is output onto an external bus in response to  
7 a read request; and  
8 storing the time delay value in the register.

C 1 <sup>28</sup>~~178~~. The method of claim <sup>27</sup>~~177~~ further including receiving a <sup>control</sup>~~set~~  
C 2 <sup>register access</sup>~~register request~~ wherein, in response to the ~~set register request~~,  
3 the register stores the time delay value.

1 <sup>29</sup>~~179~~. The method of claim <sup>28</sup>~~178~~ further including receiving the  
C 2 <sup>control register access</sup>~~set register request~~ and the time delay value in one request  
3 packet.

1 <sup>30</sup>~~180~~. An integrated circuit device having memory including at  
2 least one memory section which includes a plurality of memory  
3 cells, the integrated circuit device comprising:

4 a programmable register to store a value which is  
5 representative of a number of clock cycles of a clock to transpire  
6 before data is output onto a bus in response to a read request; and  
7 a plurality of output drivers, coupled to the bus, to output  
8 data in response to the read request, wherein the output drivers  
9 output data on the bus after the number of clock cycles of the  
10 clock transpire and synchronously with respect to the clock.

*Cont'd*  
1 <sup>31</sup>~~181~~. The integrated circuit device of claim <sup>30</sup>~~180~~ wherein the  
2 value is representative of a fraction or a whole number of clock  
3 cycles of the clock.

1 <sup>32</sup>~~182~~. The integrated circuit device of claim <sup>30</sup>~~180~~ wherein,  
2 during an initialization sequence, the programmable register stores  
3 the value.

1 <sup>33</sup>~~183~~. The integrated circuit device of claim <sup>30</sup>~~180~~ wherein the  
2 integrated circuit device stores the value in the register in  
3 response to a <sup>control register access</sup>~~set register request~~.

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